ISL70003ASEHEV2Z Evaluation Board User Guide

The ISL70003ASEHEV2Z evaluation board is designed to demonstrate the performance of the ISL70003ASEH product as a 12V input to 3.3V output, 6A output current POL regulator, with a significantly reduced size footprint compared to the ISL70003ASEHEV1Z platform, making it ideal for wiring into an existing circuit. For more detailed information, please refer to the ISL70003ASEH datasheet.

The ISL70003ASEHEV2Z evaluation board accepts a nominal input voltage of 12V and provides a regulated output voltage of 3.3V with output current ranging from 0A to 6A. There is a green LED indicating PGOOD. The input voltage and output voltage presets can be changed to alternate voltages by resistor substitutions.

The ISL70003ASEHEV2Z evaluation board is configured to run from the nominal 300kHz internal oscillator of the ISL70003ASEH.

Specifications

This board has been configured and optimized for the following operating conditions:

- 12V V_{IN}, 3.3V V_{OUT}, I_{OUT} = 6A maximum
- Power density of 9W/sq. inch of active area
- 89% peak efficiency

Key Features

- Simple to use
- Small size PCB, 2.25 sq. inches
- Power-good LED

References

ISL70003ASEH Datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL70003ASEHEV2Z	ISL70003ASEH radiation and SEE hardened 3V to 12V, 6A synchronous buck regulator evaluation board

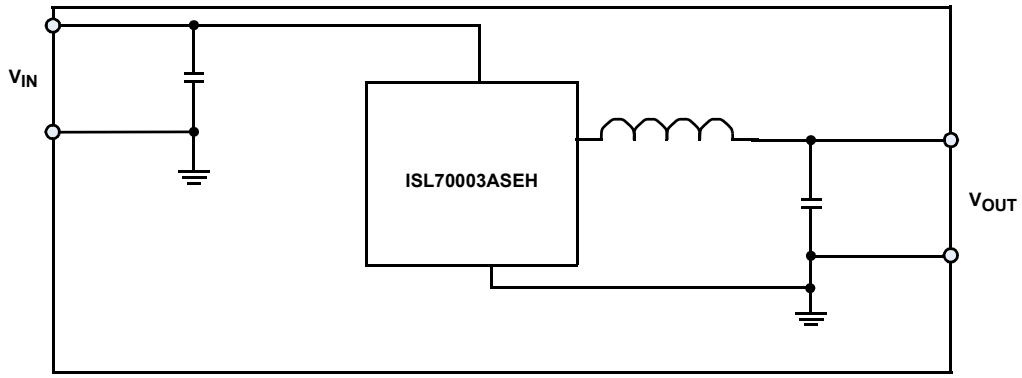

FIGURE 1. ISL70003ASEHEV2Z BLOCK DIAGRAM

ISL70003ASEHEV2Z Evaluation Board

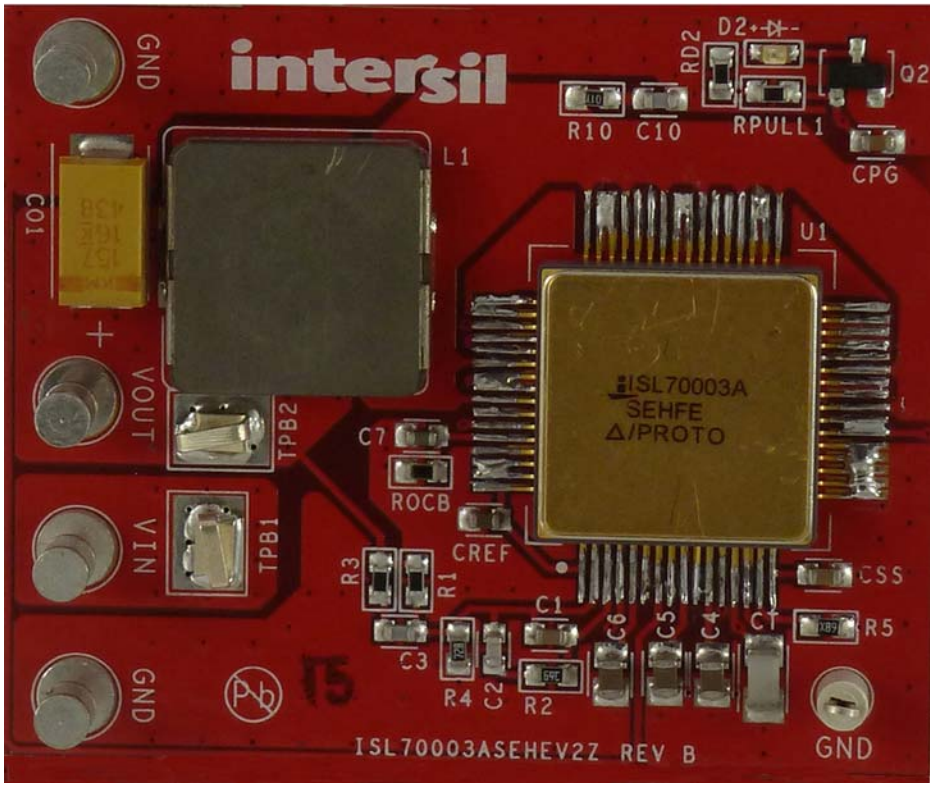

FIGURE 2. ISL70003ASEH TOP VIEW

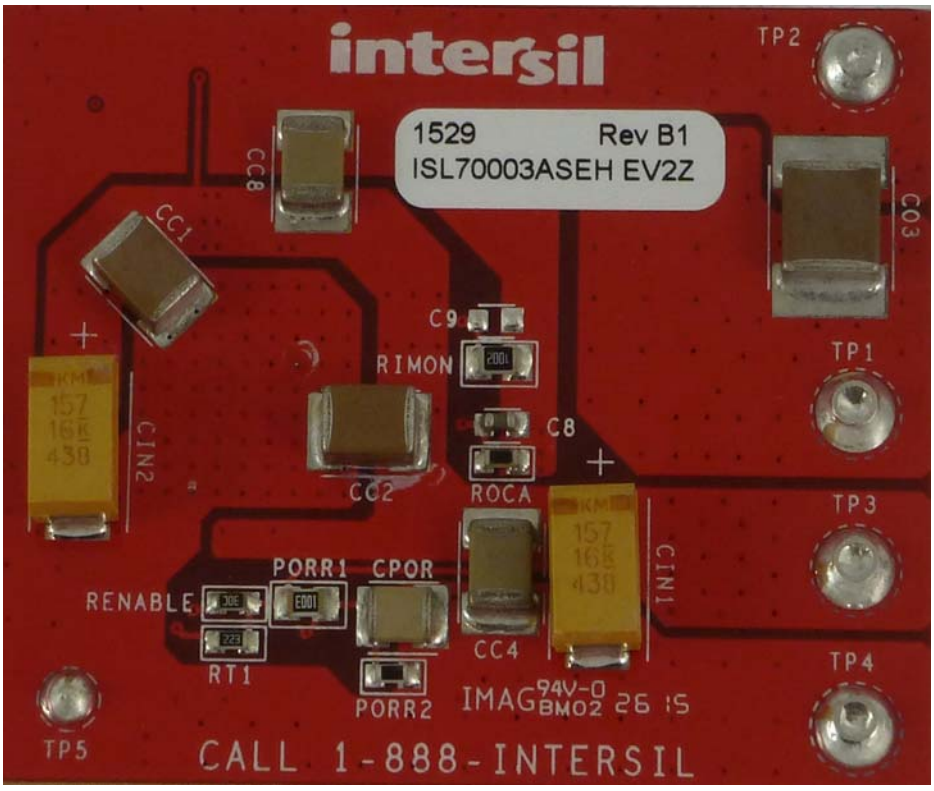

FIGURE 3. ISL70003ASEH BOTTOM VIEW

What's Inside

The evaluation board includes the following materials:

- ISL70003ASEHEV2Z evaluation board
- ISL70003ASEH Datasheet
- UG046, "ISL70003ASEHEV2Z Evaluation Board User Guide"

Recommended Test Equipment

- 12V power supply with at least 5A current capability
- Electronic load capable of sinking current to 7A
- Digital multimeters (DMMs)
- A 500MHz dual or quad trace oscilloscope

Quick Start

1. Set the power supply voltage to 12V. Connect the positive lead of the power supply to VIN and the negative lead of the power supply to GND. Turn on the power supply.
2. Connect one DMM to monitor the input voltage and another DMM to monitor the output voltage, confirm it is 3.3V.

Evaluating ISL70003ASEH

A complete evaluation of this evaluation board is easily accomplished and the user can easily change the operating points by changing resistor values. Following are simple instructions as to how to change the output voltage, the V_{IN} POR and Overcurrent Protection (OCP) thresholds to allow for a customized evaluation.

Setting Other Output Voltages

The output voltage of the regulator is programmed via an external resistor divider that is used to scale the output voltage relative to the 0.6V reference voltage. The output voltage is set for 3.3V on this circuit. To modify the output voltage, substitute R_4 for a different value according to Equation 1:

$$R_4(k\Omega) = \frac{15}{V_{OUT} - 0.6V} \quad \text{(EQ. 1)}$$

Changing the V_{IN} POR Voltage Threshold

After the EN input requirement is met, the ISL70003ASEH remains in shutdown until the voltage at the POR pin rises above its threshold. The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins. The rising POR Vth is set for ~10.2V on this circuit, see Figure 6.

The POR threshold voltage is also programmed via an external resistor divider. To modify the rising POR threshold voltage (V_{PORR}), substitute PORR2 for a different value according to Equation 2:

$$PORR2 = 100k \div \left[\left(\frac{V_{PORR} - 1.2V}{0.6}\right) - 1\right] \quad \text{(EQ. 2)}$$

Changing the Overcurrent Protection Level

The ISL70003ASEH features dual redundancy in the overcurrent detection circuitry, which helps avoid false overcurrent triggering due to single-event effects. Two external 4.02kΩ resistors (ROCA, ROCB) from pins OCSETA and OCSETB to AGND set the inductor peak current threshold at ~8.96A for the Overcurrent Protection (OCP) trip point. See Figure 8 for the relationship between the peak current sensed in the IC and the DC output current. Use Equation 3 to determine the resistor value for the desired peak inductor overcurrent protection level.

$$ROC(A/B)\ (\Omega) = \frac{36024}{I_{OCP}(A)} \quad \text{(EQ. 3)}$$

Schematic and BOM

A schematic and BOM of the ISL70003ASEHEV2Z evaluation board are shown on page 6 and page 7, respectively. The BOM shows components that are representative of the types needed for a design, but these components are not space qualified. Equivalent space qualified components would be required for flight applications.

PCB Design

PCB design is critical to high-frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Selection of a suitable thermal interface material is also required for optimum heat dissipation and to provide lead strain relief.

Optimize load regulation by reducing noise from the power and digital grounds into the analog ground by splitting ground into 3 planes; analog, digital and power. Bypass or ground pins accordingly to their design preferred ground. Independently tie each of the analog and digital grounds to power ground via a single trace in a low noise area.

PCB Plane Allocation

On the ISL70003ASEHEV2Z, four layers of two ounce copper is used as recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals, but can also provide additional power and ground islands as required. This evaluation platform is designed with 6A maximum of output current capability.

PCB Component Placement

Components should be placed as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the order shown: REF, SS, AVDD, DVDD, PVINx (high-frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the POL and the bottom leg of the divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.

When designing for >6A of output current place a Schottky clamp diode as close as possible to the LXx and PGNDx pins of the IC. A small series R-C snubber connected from the LXx pins to the PGNDx pins may be used to damp high-frequency ringing on the LXx pins if desired.

LXx Connection

Use a small island of copper to connect the LXx pins of the IC to the output inductor on layers 1 and 4. Void the copper on layers 2 and 3 adjacent to the island to minimize capacitive coupling to the power and ground planes. Place most of the island on layer 4 to minimize the amount of copper that must be voided from the ground plane (layer 2).

Keep all other signal traces as short as possible.

High Current Protection Clamp

When using the ISL70003ASEH to output current levels >6A it is highly recommended to implement a LX to PGND Schottky diode clamp to prevent damage to the lower power FET devices. The MBRS320T3G diode is used on the ISL70003ASEHEV1Z evaluation platform but is not on this evaluation platform.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads need forming to provide strain relief. On the heatsink package R64.C, the lead forming should be made so that the bottom of the heatsink and the formed leads are flush.

Heatsink Mounting Guidelines

The R64.C package has a heatsink mounted on the underside of the package. The following JESD-51x series guidelines may be used to mount the package:

1. Place a thermal land on the PCB under the heatsink.
2. The land should be approximately the same size as to 1mm larger than the 10.16x10.16mm heatsink.
3. Place an array of thermal vias below the thermal land.
   - Via array size: ~9x9 = 81 thermal vias.
   - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
   - Via pitch: ~1.2mm.
   - Vias should drop to and contact as much metal area as feasible to provide the best thermal path.

Heatsink Electrical Potential

The heatsink is connected to pin 50 within the package; thus the PCB design and potential applied to pin 50 will therefore define the heatsink potential.

Heatsink Mounting Materials

In the case of electrically conductive mounting methods (conductive epoxy, solder, etc) the thermal land, vias and connected plane(s) below must be the same potential as pin 50.

In the case of electrically nonconductive mounting methods (nonconductive epoxy), the heatsink and pin 50 could have different electrical potential than the thermal land, vias and connected plane(s) below.

Typical Performance Curves

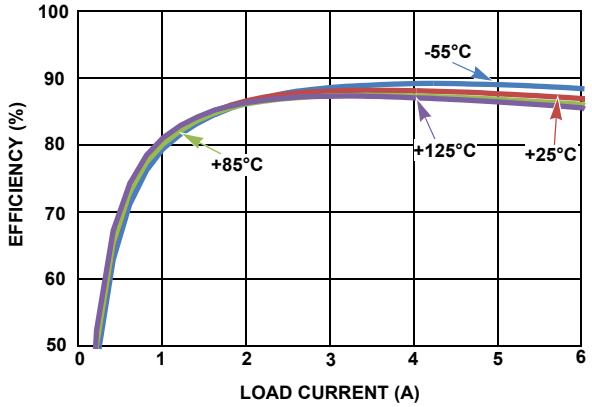

FIGURE 4. EFFICIENCY vs LOAD vs TEMPERATURE
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 300kHz

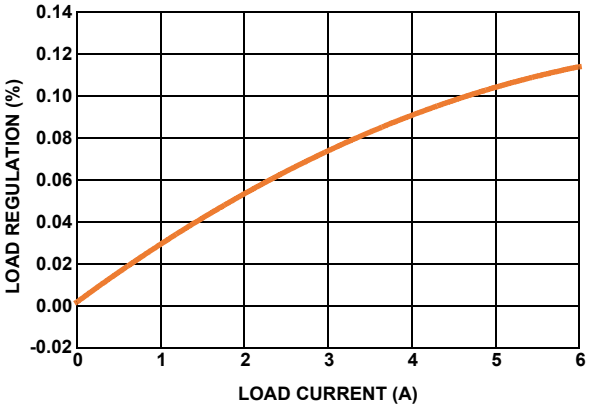

FIGURE 5. ISL70003ASEHEV2Z AMBIENT LOAD REGULATION

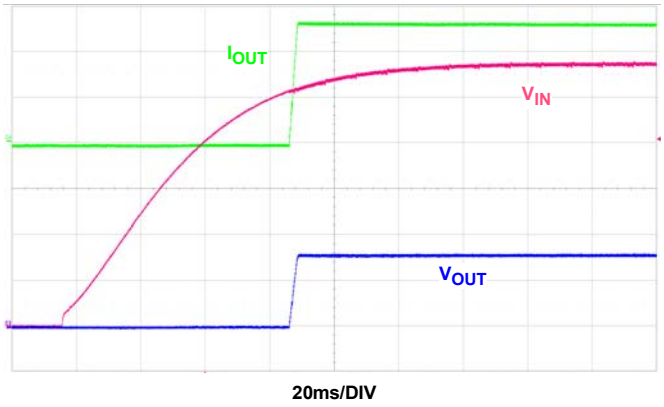

FIGURE 6. START-UP WAVEFORMS INTO 0.64Ω LOAD

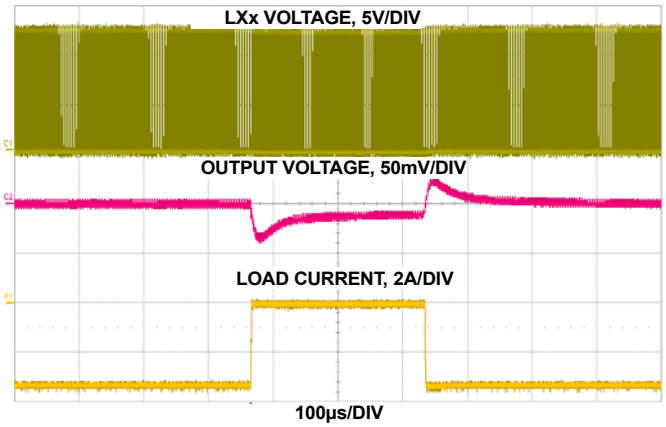

FIGURE 7. 3A LOAD TRANSIENT RESPONSE
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

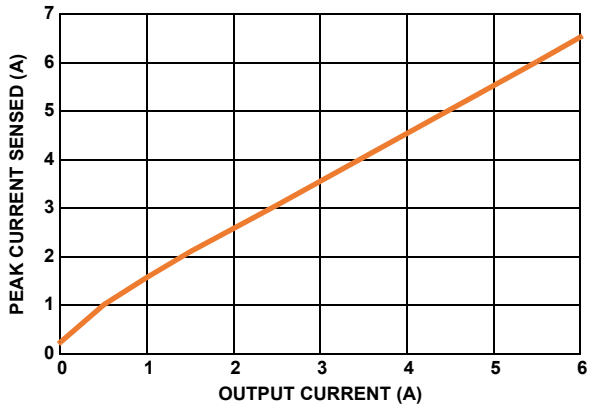

FIGURE 8. PEAK CURRENT TO DC I_{OUT}

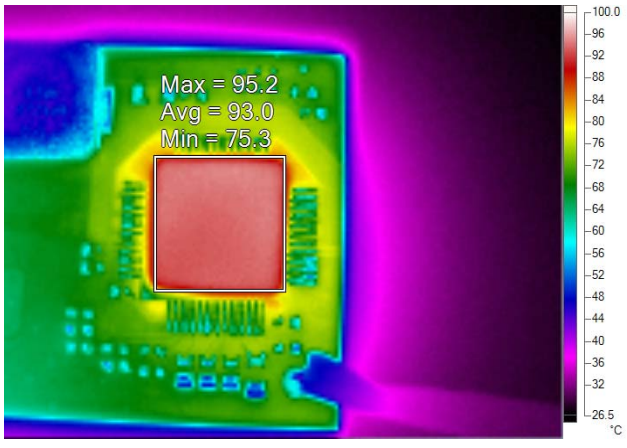

FIGURE 9. THERMAL IMAGE OF REGULATOR WITH 6A LOAD
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 300kHz, T_A = +25°C

ISL70003ASEHEV2Z Circuit Schematic

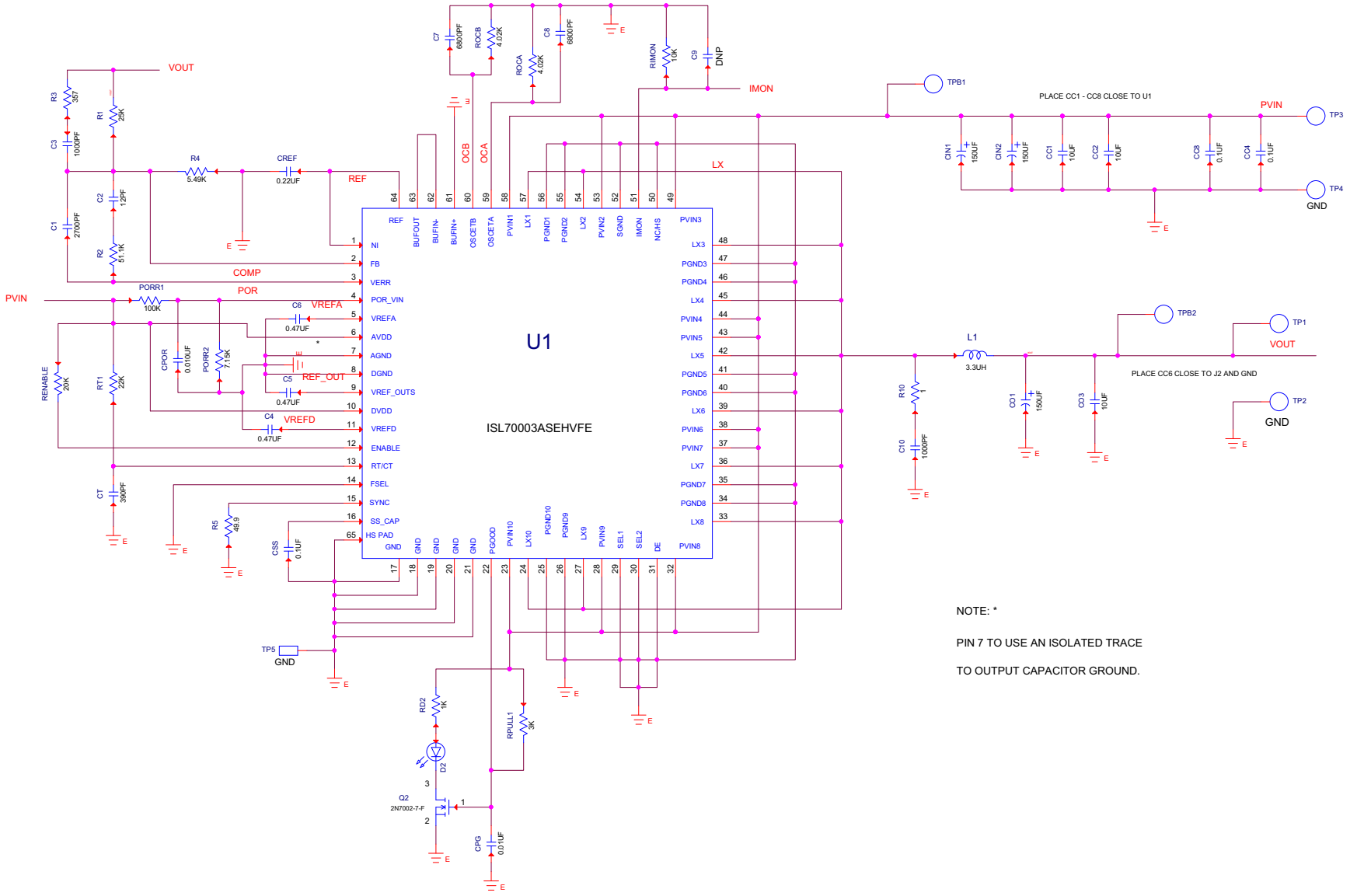

FIGURE 10. ISL70003ASEHEV2Z SCHEMATIC

Bill of Materials

REFERENCE DESIGNATOR	QTY	UNITS	DESCRIPTION	PART NUMBER	MANUFACTURER
	1	ea.	PWB-PCB, ISL70003ASEHEV2Z, REVB, ROHS	ISL70003ASEHEV2ZREVBPCB	IMAGINEERING INC
CT	1	ea.	CAP, SMD, 1206, 390pF, 50V, 1%, C0G, ROHS	12065A391FAT2A	AVX
CC1, CC2	2	ea.	CAPACITOR, SMD, 1812, 10µF, 25V, 20%, X7R	C4532X7R1E106M	TDK
CO3	1	ea.	CAPACITOR, SMD, 2220, 10µF, 25V, 20%, X7R	C5750X7R1E106M	TDK
C3, C10	2	ea.	CAP, SMD, 0603, 1000pF, 50V, 5%, C0G, ROHS	GRM1885C1H102JA01D	MURATA
CPG	1	ea.	CAP, SMD, 0603, 0.01µF, 16V, 10%, X7R, ROHS	C0603X7R160-103KNE	VENKEL
CSS	1	ea.	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	06035C104KAT2A	AVX
C2	1	ea.	CAP, SMD, 0603, 12pF, 50V, 5%, NP0, ROHS	C1608C0G1H120J	TDK
CREF	1	ea.	CAP, SMD, 0603, 0.22µF, 16V, 10%, X7R, ROHS	C1608X7R1C224K	TDK
C1	1	ea.	CAP, SMD, 0603, 2700pF, 50V, 10%, X7R, ROHS	ECJ-1VB1H272K	PANASONIC
C7,C8	2	ea.	CAP, SMD, 0603, 6800pF, 16V, 10%, X7R, ROHS	C0603X7R160-682KNE	VENKEL
C9	0	ea.	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
C4, C5, C6	3	ea.	CAP, SMD, 0805, 0.47µF, 50V, 10%, X7R, ROHS	C0805X7R500-474KNE	VENKEL
CC4, CC8	2	ea.	CAP, SMD, 1812, 0.1µF, 630V, 10%, X7R, ROHS	GRM43DR72J104KW01L	MURATA
CO1, CIN1, CIN2	3	ea.	CAP-TANT, SMD, 7.3x4.3x4.3, 150µF, 16V, 20%, 15mΩ, ROHS	T530X157M016ATE015	KEMET
CPOR	1	ea.	CAP, SMD, 1210, 0.01µF, 500V, 10%, X7R, ROHS	VJ1210Y103KXEAT5Z	VISHAY/VITRAMON
L1	1	ea.	COIL-PWR INDUCTOR, SMD, 12.9x13.2, 3.3µH, 20%, 12A, ROHS	IHLP5050CEER3R3M01	VISHAY
TP1-TP4	4	ea.	CONN-TURRET, TERMINAL POST, TH, ROHS	1514-2	KEYSTONE
TP5	1	ea.	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	5002	KEYSTONE
TPB1, TPB2	2	ea.	CONN-COMPACT TEST POINT, SMD, ROHS	5016	KEYSTONE
D2	1	ea.	LED, SMD, 0603, GREEN CLEAR, 2V, 20mA, 571nm, 35mcd, ROHS	LTST-C190KGKT	LITEON/VISHAY
U1	1	ea.	IC-RAD-HARD BUCK REGULATOR, 64P, CQFP, CLASS V, ROHS	ISL70003ASEHVFE	INTERSIL

Bill of Materials (Continued)

REFERENCE DESIGNATOR	QTY	UNITS	DESCRIPTION	PART NUMBER	MANUFACTURER
Q2	1	ea.	TRANSISTOR,N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	2N7002-7-F	DIODES, INC.
RT1	1	ea.	RES, SMD, 0603, 22k, 1/10W, 0.1%, 25ppm, THINFILM, ROHS	ERA-3AEB223V	PANASONIC
ROCA, ROCB	2	ea.	RES, SMD, 0603, 4.02k, 1/10W, 0.1%, 25ppm, ROHS	MCT06030D4021BP500	VISHAY
R10	1	ea.	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	ERJ-3RQF1R0V	PANASONIC
RD2	1	ea.	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	ERJ-3EKF1001V	PANASONIC
RENABLE	1	ea.	RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS	CR0603-10W-2002FT	VENKEL
R1	1	ea.	RES, SMD, 0603, 24.9k, 1/10W, 1%, TF, ROHS	ERJ-3EKF2492V	PANASONIC
RPULL1	1	ea.	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	RC0603FR-073KL	YAGEO
R3	1	ea.	RES, SMD, 0603, 357Ω, 1/10W, 1%, TF, ROHS	ERJ-3EKF3570V	PANASONIC
R5	1	ea.	RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS	CR0603-10W-49R9FT	VENKEL
R2	1	ea.	RES, SMD, 0603, 51.1k, 1/10W, 1%, TF, ROHS	CR0603-10W-5112FT	VENKEL
R4	1	ea.	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	CR0603-10W-5491FT	VENKEL
PORR2	1	ea.	RES, SMD, 0603, 7.15k, 1/10W, 1%, TF, ROHS	ERJ-3EKF7151V	PANASONIC
RIMON	1	ea.	RES, SMD, 0805, 10k, 1/8W, 1%, TF, ROHS	CR0805-8W-1002FT(PbFREE)	VENKEL
PORR1	1	ea.	RES, SMD, 0805, 100k, 1/8W, 1%, TF, ROHS	CR0805-8W-1003FT	VENKEL
Place assy in bag	1	ea.	BAG, STATIC, 3x5, ZIP LOC	D810 (212403-012)	INTERSIL COMMON STOCK
AFFIX TO BACK OF PCB	1	ea.	LABEL-DATE CODE_LINE 1: YRWK/REV#, LINE 2: BOM NAME	LABEL-DATE CODE	INTERSIL

Board Layout

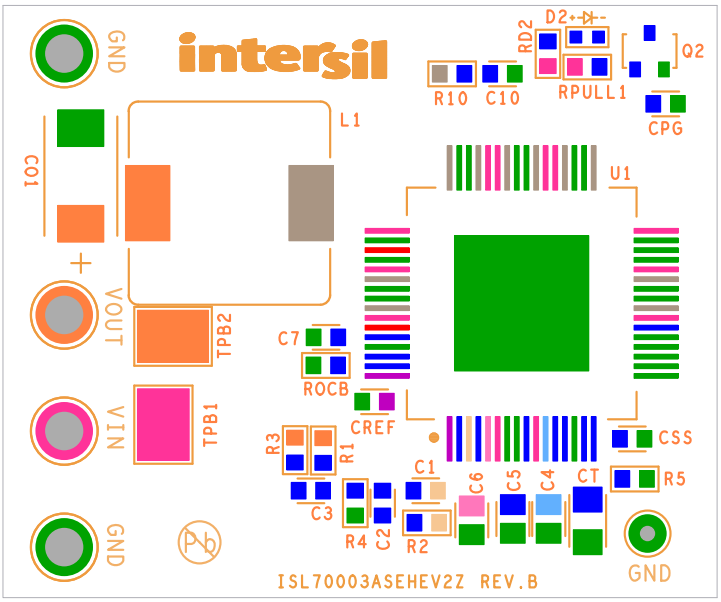

FIGURE 11. TOP SILKSCREEN LAYER

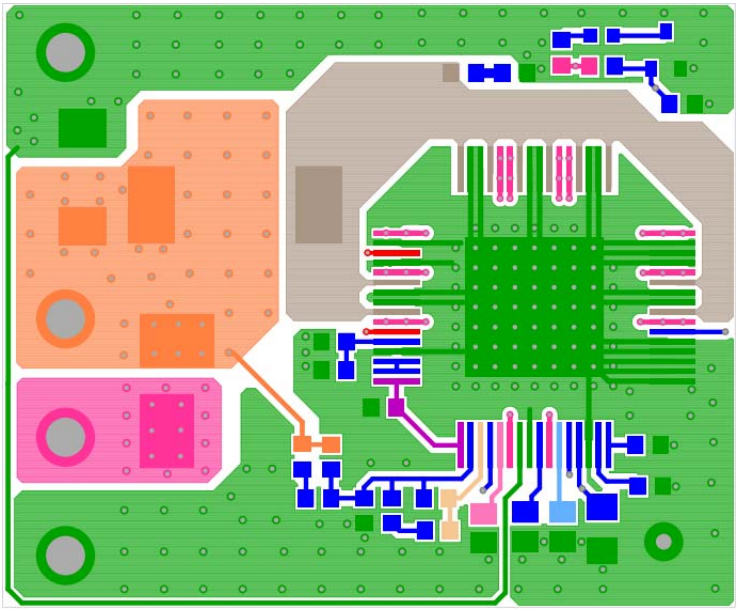

FIGURE 12. TOP COMPONENT PLACEMENT LAYER

Board Layout (Continued)

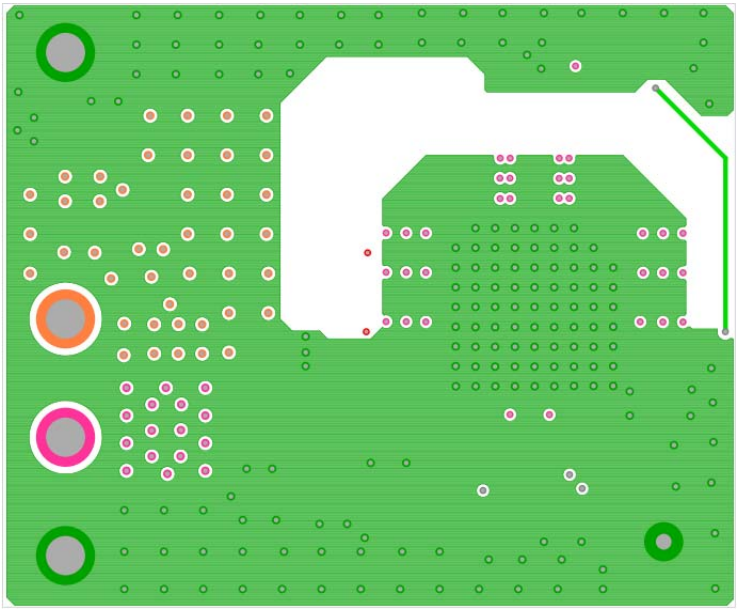

FIGURE 13. LAYER 2

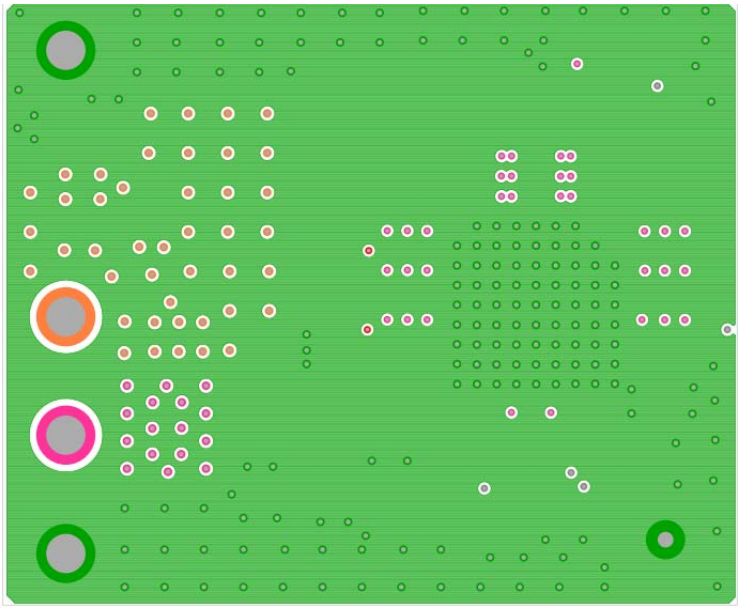

FIGURE 14. LAYER 3

Board Layout (Continued)

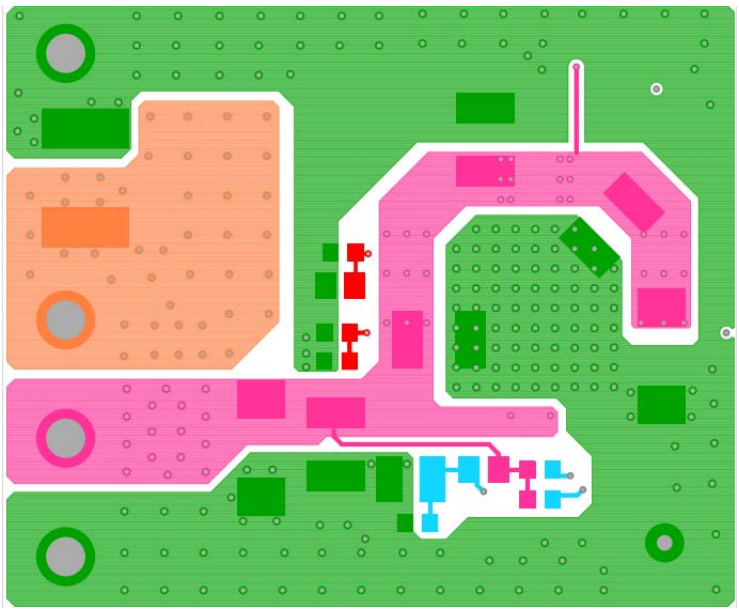

FIGURE 15. BOTTOM COMPONENT LAYER

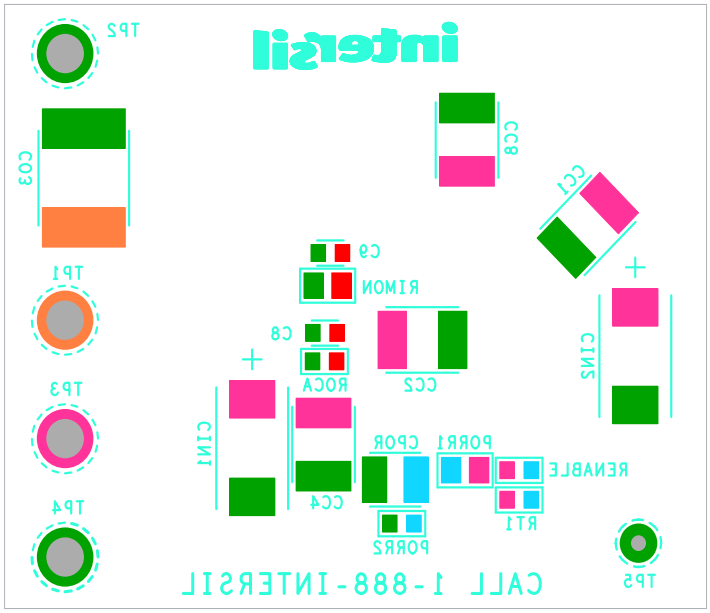

FIGURE 16. BOTTOM SILK SCREEN LAYER